IN THE CLAIMS:

Claim 1: (**Currently Amended**) A microprocessor to which a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which carries out a first address conversion by assigning ~~assigns~~ a first physical address of said a first memory said unit ~~out of said plurality of memory units~~ to a first logical address of a load module stored in a said first memory unit, wherein said load module includes an instruction code ~~instructions~~ and numerical data;

a copying unit which copies said ~~an~~ instruction code from said load module stored in said first memory unit to said a second memory unit out of said plurality of memory units; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning ~~assigns~~ a second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical addressed ~~assigned with said physical address of said first memory unit~~, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address ~~assigned with said physical address of said second memory unit~~.

Claim 2. (**Original**) The microprocessor according to claim 1, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

Claim 3. (**Original**) The microprocessor according to claim1, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

Claim 4. (**Currently Amended**) A microprocessor to which a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other are externally connected, said microprocessor comprising:

a first address conversion unit which carries out a first address conversion by assigning ~~assigns~~ a first physical address of said a first memory unit ~~out of said plurality of memory units~~ to a first logical address of a load module stored in a said first memory unit, wherein said load module include an instruction code ~~instructions~~ and numerical data;

a processing unit which temporarily stores and copies said ~~an~~ instruction code from said load module stored in said first memory unit to said a second memory unit ~~out of said plurality of memory units~~; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning ~~assigns~~ a second physical address of

said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address ~~assigned with said physical address of said first memory unit~~, and

said second address conversion unit comprises a second comparator said requested logical address with said second logical address ~~assigned with said physical address of said second memory unit~~.

8 ~~6~~. (**Original**) The microprocessor according to claim 7 ~~4~~, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said second memory unit to said logical address of the instruction code from said load module to be accessed.

9 ~~6~~. (**Original**) The microprocessor according to claim 7 ~~4~~, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

12 ~~7~~. (**Currently Amended**) A memory device comprising:

a plurality of memory units including a first memory unit including a first memory unit and a second memory unit and having physical addresses different from each other;

a first address conversion unit which carries out a first address conversion by assigning ~~assigns~~ a first physical address of said a first memory unit ~~out of said plurality of memory units~~ to a first logical address of a load module stored in said first memory unit, wherein said load module includes an instruction code ~~instructions~~ and numerical data;

a copying unit which copies said ~~an~~ instruction code from said and instruction code from said load module stored in said first memory unit to said a second memory unit ~~out of said plurality of memory units~~; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning ~~assigns~~ a second physical address of said second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address ~~assigned with said physical address of said first memory unit~~, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address ~~assigned with said physical address of said second memory unit~~.

Claim 13. (**Original**) The memory device according to claim 12, wherein when said load module stored in said second memory unit is accessed, said first address conversion unit assigns the physical address of said first memory unit to the logical address of said load module to be accessed, and said second address conversion unit assigns the physical address of said

second memory unit to said logical address of the instruction code from said load module to be accessed.

Claim 14. (**Original**) The memory device according to claim 12, wherein said load module stored in said first memory unit includes data for image processing and the instruction codes for image processing.

Claim 15. (**Original**) The memory device according to claim 12, wherein the access speed of said second memory unit is faster than the access speed of said first memory unit.

Claim 16. (**Original**) The memory device according to claim 15, wherein said second memory unit is constituted of a synchronous DRAM.

Claim 19. (**Currently Amended**) A memory device comprising:

a plurality of memory units including a first memory unit and a second memory unit and having physical addresses different from each other;

a first address conversion unit which carries out a first address conversion by assigning ~~assigns~~ a first physical address of said a first memory unit out of said plurality of memory units to a first logical address of a load module stored in said first memory unit, wherein said load module includes an instruction code ~~instructions~~ and numerical data;

a processing unit which temporarily stores and copies said ~~an~~ instruction code from said load module stored in said first memory unit to said a second memory unit ~~out of said plurality of memory units~~; and

a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning ~~assigns~~ a second physical address of said second memory unit to a second logical address of the instruction code copied to said second memory unit, wherein

said first address conversion unit comprises a first comparator that compares a requested logical address with said first logical address assigned with said physical address of said first memory unit, and

said second address conversion unit comprises a second comparator that compares said requested logical address with said second logical address ~~assigned with said physical address of said second memory unit~~.

Claim 18. (**Canceled**)

Claim ~~19~~ 5. (**New**) The microprocessor according to claim 1, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

Claim ~~20~~ 6. (**New**) The microprocessor according to claim 1, wherein the second address conversion unit carries out the second address conversion for the instruction code.

Claim ~~21~~ 10. (**New**) The microprocessor according to claim ~~4~~ 7, wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

Claim 11 (~~22~~). **(New)** The microprocessor according to claim 7 (~~4~~), wherein the second address conversion unit carries out the second address conversion for the instruction code.

Claim 17 (~~23~~). **(New)** The memory device according to claim 12 (~~7~~), wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

Claim 18 (~~24~~). **(New)** The memory device according to claim 12 (~~7~~), wherein the second address conversion unit carries out the second address conversion for the instruction code.

Claim 24 (~~25~~). **(New)** The memory device according to claim 19 (~~12~~), wherein the first address conversion unit carries out the first address conversion for information including the numerical data.

Claim 25 (~~26~~). **(New)** The memory device according to claim 19 (~~12~~), wherein the second address conversion unit carries out the second address conversion for the instruction code.